REMARKS

Claim 3 is rejected as indefinite. Claims 1-3, 12-13, 23-25, and 37-38 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Pat. to Wollan et al.[1] ("Wollan").

Claims 3, 12, 25, and 37 have been amended. Applicant respectively traverses the rejections.

A. Claim 1 comprises (a)-(g).

According to the Office Action, (a) and (b) are disclosed at Wollan col. 4, lines 20-28, which discloses 16-bit busses 14 and 16 for addressing a 16-bit address space.[2] However, the cited material does not disclose structure for addressing "up to 2^M memory locations" with a "dedicated bus . . . having N data lines, where M is greater than N."[3] Thus, (a) and (b) are not anticipated by Wollan col. 4, lines 20-28.

According to the Office Action, (c) and (d) are also disclosed at Wollan col. 4, lines 20-28. Applicant's remarks with regard to (a) and (b) are also applicable to (c) and (d). Thus, (c) and (d) are not anticipated by Wollan col. 4, lines 20-28.

According to the Office Action, (e) is taught by Wollan col. 4, line 62 to col. 5 line 5. However, the cited material does not disclose performing a first data cycle if the first and second address portions, when combined, form a first address. Thus, (e) is not anticipated by Wollan col. 4, lines 20-28.

According to the Office Action, (f) is "equivalent to a write cycle when the microcontroller is using the 8-bit mode of operation" as disclosed by Wollan FIG. 1. However, FIG. 1 does not disclose modes of operation. Thus, (f) is not anticipated by Wollan FIG. 1.

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[1] No. 5,809,327
[2] Col. 2, lines 22-24.
[3] Preamble claim 1.

According to the Office Action, (g) is "equivalent to a write cycle when the microcontroller is using the 16-bit mode of operation" as disclosed at Wollan col. 6, line 63 to col. 7, line 4. However, the cited material does not disclose that "the second address cycle is immediately subsequent to the first address cycle, and the first data cycle is immediately subsequent to the second address cycle." Thus, (g) is not anticipated by Wollan col. 6, line 63 to col. 7, line 4.

B. Claims 2-3 depend from claim 1 are not anticipated for at least the same reasons that claim 1 is not anticipated.

C. Amended claim 12 recites "at least two registers . . . each register associated with a particular count of address-bytes received on a dedicated bus for coupling the device and a processor," which according to the Office Action is disclosed at Wollan col. 3, line 59 to col. 4, line 46. However, the cited material does not disclose a register that is associated with a particular count of address-bytes received on a dedicated bus. Nor does the cited material disclose a dedicated bus that couples that device and a processor, the bus having N data lines and at least two control lines, where M is greater than N. Thus, the "at least two registers . . . " are not anticipated by Wollan col. 3, line 59 to col. 4, line 46.

Amended claim 12 recites "a unit to monitor control signals placed on the bus by the processor," which according to the Office Action is disclosed at Wollan col. 4, lines 29-46. However, the cited material does not disclose a device coupled with a processor having such a unit. Thus, "a unit to monitor control signals placed on the bus by the processor" is not anticipated by Wollan at col. 3, line 59 to col. 4, line 46.

Amended claim 12 recites "(a) a . . . counter to count address-bytes *received on the bus* by counting each assertion of an address transfer signal,"[4] which according to the Office Action is disclosed at Wollan col. 4, lines 29-46. However, the cited material does not disclose a device coupled with a processor that monitors address-bytes received by the device. Nor does the cited material disclose a device that counts address transfer signals placed on the bus by the processor. Thus, (a) is not anticipated by Wollan col. 4, lines 29-46.

Amended claim 12 recites "(b) a selecting unit to select one of the at least two registers according to a count of the address-byte-received counter," which according to the Office Action is disclosed at Wollan col. 4, lines 29-46. However, the cited material does not disclose structure in a device coupled with a processor for selecting a register based on a count of address transfer signals placed on the bus by the processor. Thus, (b) is not anticipated by Wollan col. 4, lines 29-46.

Amended claim 12 recites "(c) first logic to store an address-byte received on the bus . . . in response to *detecting an assertion of the address transfer signal*,"[5] which according to the Office Action is disclosed at Wollan col. 4, lines 29-46 and col. 10, lines 28-64. However, the cited material does not disclose structure in a device coupled with a processor for storing an address-byte received on the bus in response to detecting an assertion of the address transfer signal by the processor. Thus, (c) is not anticipated by Wollan col. 4, lines 29-46 and col. 10, lines 28-64.

Amended claim 12 recites "(d) second logic . . . to reset the address-byte received counter . . . ," which according to the Office Action is *inherently* disclosed in Wollan. However, Wollan does not disclose structure in a device coupled with a processor to reset an address-byte received counter. Thus, (d) is not inherently anticipated by Wollan.

[4] Emphasis added.
[5] Emphasis added.

D. Claim 13 depends from claim 12 and is not anticipated for at least the same reasons that claim 12 is not anticipated.

E. Claim 23 comprises (a)-(g).

According to the Office Action, (a) and (b) are disclosed at Wollan col. 4, lines 20-28, which discloses 16-bit busses 14 and 16 for addressing a 16-bit address space.[6] However, the cited material does not disclose structure for addressing "up to 2^M memory locations" with a "dedicated bus . . . having N data lines, where M is greater than N."[7] Thus, (a) and (b) are not anticipated by Wollan col. 4, lines 20-28.

According to the Office Action, (c) and (d) are also disclosed at Wollan col. 4, lines 20-28. Applicant's remarks with regard to (a) and (b) are also applicable to (c) and (d). Thus, (c) and (d) are not anticipated by Wollan col. 4, lines 20-28.

According to the Office Action, (e) is taught by Wollan Table I, in col. 12, which summarizes thirty-two different control lines in the microcontroller. However, the cited table does not disclose performing a first data cycle if the first and second address portions, when combined, form a first address. Thus, (e) is not anticipated by Wollan Table I, in col. 12.

According to the Office Action, (f) is "equivalent to a write cycle when the microcontroller is using the 8-bit mode of operation" as disclosed by Wollan FIG. 1. However, FIG. 1 does not disclose modes of operation. Thus, (f) is not anticipated by Wollan FIG. 1.

According to the Office Action, (g) is "equivalent to a write cycle when the microcontroller is using the 16-bit mode of operation" as disclosed at Wollan col. 6,

[6] Col. 2, lines 22-24.
[7] Preamble claim 1.

line 63 to col. 7, line 4. However, the cited material does not disclose that "the second address cycle is immediately subsequent to the first address cycle, and the first data cycle is immediately subsequent to the second address cycle." Thus, (g) is not anticipated by Wollan col. 6, line 63 to col. 7, line 4.

F. Claims 24-25 depend from claim 23 and are not anticipated for at least the same reasons that claim 23 is not anticipated.

G. Applicant assumes that section 12 of the Office Action pertains to claim 37 not claim 23.

Claim 37 recites "a system, comprising: a central processing unit, a device," and a "bus to exclusively couple the central processing unit and the device. According to the Office Action, the "central processing unit" is disclosed in Wollan Figure 1 with support at col. 3, lines 59-65, and the bus is disclosed in Wollan Figure 1. However, Figure 1 with support in claim 1 discloses that the bus referred to at col. 3, lines 59-65 is an element or component of the central processing unit of Figure 1. In addition, Wollan discloses that various components of the "device" are also disclosed as an element or component of the central processing unit of Figure 1. The finding in the Office Action that Figure 1 discloses a central processing unit is inconsistent with the findings that Figure 1 discloses a device and a bus. Claim 37 is not anticipated by Wollan at least for the reason that Wollan does not disclose a system comprising a device and a bus; Figure 1 discloses only one of the claimed elements, namely the central processing unit.

Claim 37 is also not anticipated at least for the reasons stated above with respect to the device claimed in claim 12. Claim 12 employs language similar to that found in claim 37.

H. Claim 38 depends from claim 37 and is not anticipated for at least the same reasons that claim 37 is not anticipated.

I. General Remarks

1. MPEP 2131 provides:

"'A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) . . . 'The identical invention must be shown in as complete detail as is contained in the . . . claim.' *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim . . . *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

2. Wollan discloses an eight-bit data bus 12, a RAM, and a REGISTER FILE 20. The registers "in the register file occupy a portion of the address space of the RAM."[8] According to Wollan,

"the REGISTER FILE . . . includes register circuitry 100 which provides thirty-two eight bit registers R0-R31 . . . the register circuitry 100 is capable of provisioning the last six registers R26-R31 as three pairs of logical sixteen bit registers . . . (X), . . . (Y), . . . (Z)."[9]

The register circuitry 100 includes "selector control circuitry 134." Control lines "R_SEL and WE_R" coupled with the selector control circuitry 134 cooperate to write data to a selected register.

"the bank of eight flip-flops corresponding to each register R0-R31 is written to by presenting input to the D leads and by asserting the clock lines CK of the flip-flops . . . the selector control circuitry 134 . . . asserts the proper CK signals so that the correct register and bit(s) are written. The R_SEL and WE_R control lines cooperate to write the eight flip-flops corresponding to a selected register."[10]

[8] Wollan, col. 2, lines 61-63.
[9] Wollan, col. 4, line 62 to col. 5, line 2.
[10] Wollan, col. 6, lines 29-44.

The selector control circuitry 134 determines which register to select using a decoder unit 140. "The decoder unit 140 is a 1:32 decoder which asserts any one of the 32 output[s] in response to decoding R_SEL. Each output line of the decoder corresponds to a register."[11]

"Consider, for example, the writing of data into register R0. The five bit control line R_SEL is set to select register R0. The decoder 140 decodes the line, thereby asserting the output line corresponding to register R0."[12]

Thus, R_SEL is a 5-bit control line used to select a particular register R0-R31 when writing data to the REGISTER FILE 20.

Wollan discloses that the value placed on a control line, such as R_SEL, is determined by a software instruction. For example, the LD instruction may be used to transfer data stored in the RAM to a selected register. Another example of a software instruction determining a control line value is the ST instruction, which may be used to transfer the contents of a selected register to a memory location in the RAM. The ST instruction determines the value of the 5-bit R_OUTC control line rather than the R_SEL control line.

"Operations on the sixteen-bit X, Y, Z registers include the LD instruction for transferring data to a specified register from a memory location addressed by an X, Y, Z register; and the ST instruction for transferring data from a specified register to a memory location addressed by an X, Y, Z register. The LD and ST instructions require two clock cycles to execute. Referring to FIGS. 2 and 3, during the first clock cycle, the R_OUTA and R_OUTB control lines select the register pair of the desired sixteen-bit register (X:R27/R26, Y:R29/R28, Z:R/31/R30). The ADDR_SEL control line operates selector 114 to place the B:A outputs onto the indirect address bus 14. Additionally, in the case of an ST instruction, the R_OUTC control line selects the register from which the data is to be read, placing the data on the bus 12. During the second clock cycle, the memory is strobed either to load data from memory onto the bus 12 (LD) or to write data into memory (ST). Additionally, in

[11] Wollan, col. 7, lines 6-9.
[12] Wollan, col. 7, lines 52-54.

the case of an LD instruction, the R_SEL an[d] WE_R control lines are selected to write data from D_BUS into the specified the register."[13]

Moreover, one of ordinary skill in the art would appreciate that the Wollan software instructions include operands that define the address of the selected register. This conclusion is supported by the documentation published by the Assignee of the Wollan patent attached hereto as Exhibit A. Exhibit A includes excerpts from Microcontroller documentation and Instruction Set documentation. This documentation is consistent with the Wollan application in numerous respects. The Microcontroller documentation describes an 8-bit RISC microcontroller which uses the Harvard architecture and which is designed around an 8-bit data bus. In addition, the Microcontroller documentation uses a block diagram similar to that found Wollan Figure 1. As mentioned, Wollan discloses that the registers "in the register file occupy a portion of the address space of the RAM." Consistent with Wollan, the Microcontroller documentation discloses a register file having registers R0-R31 and shows assigned register addresses within an SRAM data memory. Also consistent with Wollan, the Microcontroller documentation includes a timing diagram showing that both data and address lines are involved in a memory accesses. The instruction set documentation includes many of the same instructions disclosed in Wollan, e.g., the LD and ST instructions. The LD instruction requires specification of a destination register in the register file (Rd) and one of the indirect registers in the register file (X). Similarly, the ST instruction requires specification of a source register in the register file (Rr) and one of the indirect registers in the register file (X). Thus, these documents support the conclusion that one of ordinary skill in the art would understand that the Wollan software instructions include operands that define the address of the selected register.

3. One of ordinary skill in the art would understand that the Wollan operations for reading or writing to a memory location are performed differently from those claimed. Moreover, even though some of the same elements may be

[13] Wollan, col. 14, lines 46-65.

included in both Wollan and the claims, because the claimed inventions operate differently from Wollan, one of ordinary skill would appreciate that the Wollan elements are not arranged as required by the claim. In addition, Wollan fails to disclose each and every element as set forth in the claims.

First, Wollan discloses that memory access operations require presenting the memory with an address on a 16-bit address bus. Simultaneously, data is presented to the memory or sampled from the memory on an 8-bit data bus. In contrast, the claims recite memory access operations that include presenting address and data sequentially on a single bus having a bus-width insufficient to define all addresses in the address space. Thus, the Wollan operations are performed differently from those claimed.

Moreover, the Wollan registers are accessed using register addresses. Because each register is identified with an address, any of the 32 disclosed registers can be randomly identified in one clock cycle. In contrast, the claimed registers are identified by a sequential count of address cycles. In certain claims, two address cycles are required to identify the second register. In other claims, three address cycles are required to identify a third register. The claims do not require that the registers be defined in the address space of the memory nor do they inherently require that a software instruction identify an address of a selected register. Thus, the Wollan operations are performed differently from those claimed.

Second, Wollan discloses a bus configuration which is different from that claimed. Wollan discloses distinct busses for address and data. The Wollan data bus is 8-bits wide. In one embodiment, the Wollan address bus is 16-bits wide. The Wollan 16-bit indirect address bus 14 is connected between the register file, the RAM, and the program counter. The Wollan 8-bit data bus is connected between the register file and the RAM. The Wollan 8-bit data bus is <u>not</u> connected to the program counter. In contrast, a single bus to couple the CPU and the device is claimed. The single bus has N data lines where M is greater than M and is used to

access 2^M memory locations. The single bus is used for both address and data. Plainly, the only bus in Wollan that one of ordinary skill in the art would analogize to the claimed bus is the Wollan data bus 12. But Wollan data bus 12 is not coupled with the Wollan program counter. Thus, one of ordinary skill would not conclude that the Wollan data bus 12 anticipates the claimed bus. Accordingly, the Wollan elements are not arranged as required by the claim contrary to the requirement of *In re Bond*.

Third, Wollan fails to disclose each and every element as set forth in the claims. For example, amended claim 12 recites "a unit to monitor control signals placed on the bus by the processor, the unit including: (a) a K-bit address-byte-received counter to count address-bytes received on the bus by counting each assertion of an address transfer signal on a first control line." Wollan discloses no corresponding structure. In addition, claim 37 recites language similar to the above-quoted language from claim 12 and with respect to claim 12 Wollan fails to disclose corresponding structure. For at least these reasons, Wollan fails to disclose each and every element as set forth in the claims.

Conclusion

Accordingly, claims 1-3, 12-13, 23-25, and 37-38 are in condition for allowance. Applicant respectively requests that claims 1-3, 12, 23-25, and 37 be allowed, and this application be passed to issue. Should the Examiner feel that a telephone conference would expedite prosecution of this application, the Examiner is invited to call Applicant's attorney, Richard A. Wilhelm (48,786), at (503) 635-1187.

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